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Mask Substrate Requirements and Development for Extreme Ultraviolet Lithography (EUVL)

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Mask substrate requirements and development for extreme ultraviolet lithography (EUVL)

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ABSTRACT

The mask is deemed one of the areas that require significant research and development in EUVL. Silicon wafers will be used for mask substrates for an alpha-class EUVL exposure tool[†] due to their low-defect levels and high quality surface finish. However, silicon has a large coefficient of thermal expansion that leads to unacceptable image distortion due to absorption of EUV light. A low thermal expansion glass or glass-ceramic is likely to be required in order to meet error budgets for the 70nm node and beyond. Since EUVL masks are used in reflection, they are coated with multilayers prior to patterning. Surface imperfections, such as polishing marks, particles, scratches, or digs, are potential nucleation sites for defects in the multilayer coating, which could result in the printed defects. Therefore we are accelerating developments in the defect reduction and surface finishing of low thermal expansion mask substrates in order to understand long-term issues in controlling printable defects, and to establish the infrastructure for supplying masks. In this paper, we explain the technical requirements for EUVL mask substrates and describe our efforts in establishing a SEMI standard for EUVL masks. We will also report on the early progress of our suppliers in producing low thermal-expansion mask substrates for our development activities.

Keywords: EUVL, mask substrate, mask format, mask material

1. INTRODUCTION

Extreme Ultraviolet Lithography (EUVL) is a leading candidate for the Next Generation Lithography (NGL) for fabricating semiconductor microelectronics.[1] EUVL technology development is progressing toward insertion into the production of integrated circuits with critical dimensions (CD) of 70nm. The key difference between EUVL and conventional lithography is that EUVL employs 13.4nm light and therefore requires reflective optics that are coated with multilayers (ML), typically Mo/Si. The feasibility of creating features down to 70nm has been established using small-field EUVL printing tools,[2,3] and development efforts are currently underway to demonstrate that cost effective production equipment can be engineered to perform full width ring-field imaging consistent with high wafer throughput rates. An alpha-class tool, called the Engineering Test Stand (ETS), is planned for completion in Y2001 (Figure 1)[4]. Experiments performed with the ETS will demonstrate that the key technologies necessary for implementing EUVL are well understood and that all key development issues have been addressed. The ETS is a ring-field scanning system, where an arc-shaped region of the mask is imaged with a reduction of 4x onto an arc shaped region on the wafer. Stages for both the mask and the wafer are scanned in order to print the entire field.

An enabling technology for EUVL is the high reflectivity ML coating.[5] Deposition of low defect, uniform ML coatings for the mask blanks is an area of intense development at the EUV Virtual National Laboratory (VNL), and its progress is being reported in these proceedings by Burkhart *et al.* This paper focuses on the technical requirements and the progress of development for EUVL mask substrates.

Mask substrates for the ETS will initially be fabricated on epi-silicon wafers because they exhibit the lowest defect levels and surface roughness of the available substrate materials to date. Epi-silicon wafers are produced by depositing 1-3μm of epitaxial silicon on a polished wafer that has been intentionally oriented by less than 1° away from the (100) crystallographic direction. This creates evenly spaced terraces on the surface and ensures that subsequent silicon deposition will proceed in the "step-flow" mode, which minimizes the roughening of the surface. The epi-silicon layer heals surface defects produced in crystal growth and chemical mechanical polishing (CMP) processes. Figure 2 shows an AFM scan of a

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† The Engineering Test Stand (ETS) is being constructed by collaboration between the EUV LLC and the Virtual National Laboratory (Lawrence Livermore, Sandia, and Lawrence Berkeley National Laboratories).

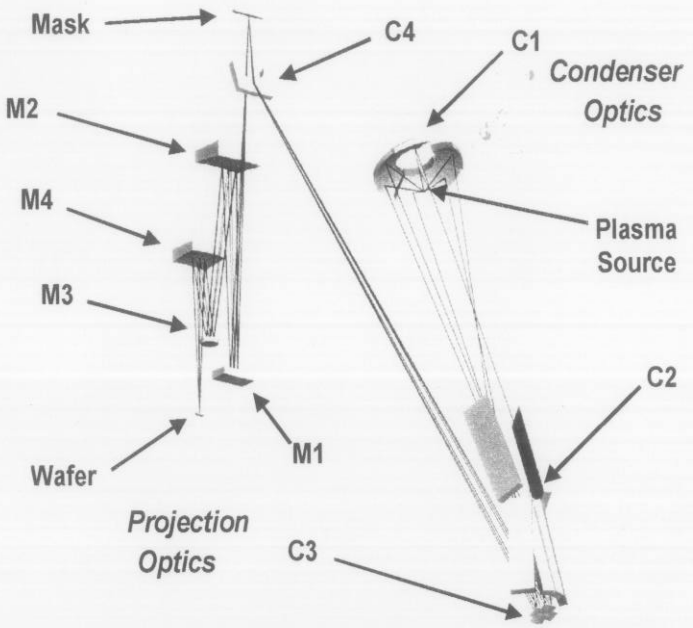


Figure 1. Schematic of the optical system for the ETS that employs a 4-mirror, 4x reduction camera.

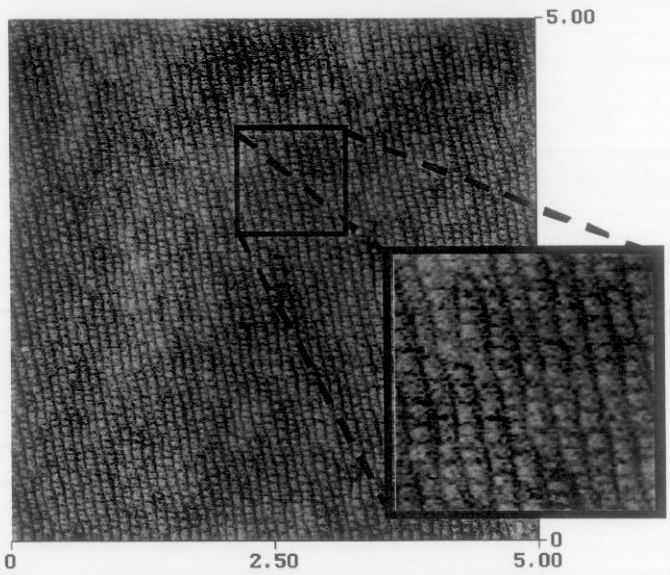


Figure 2. AFM scan of epi-Si(100) surface with atomic terraces of about 0.07nm in height. The roughness of this surface is <0.1nm rms.

typical epi-Si(100) surface with its characteristic atomic terraces. The surface has a roughness of <0.1nm rms, which is common for the silicon wafers we use.

The overlay requirements of sub-100 nm lithography preclude the use of materials with a high coefficient of thermal expansion (CTE) for EUVL mask substrates because a high CTE will lead to an unacceptable image displacement error when the mask is illuminated during printing. Silicon substrates will be utilized initially but will be replaced by a low thermal expansion (LTE) material, either a glass or a glass-ceramic as they become available. The silicon wafer represented the "best" surface for EUVL mask applications and will be the standard against which all future LTE substrates will be compared; in order for the LTE glass substrates to be adopted, their figures of merit must approach those for silicon. ULE®‡, which is an LTE glass composed of amorphous SiO_2 doped with about 7% TiO_2, was selected as the primary candidate for mask substrate because one of our vendors had succeeded in producing ULE substrates with <0.1nm rms roughness on 1-inch optical flat format. Zerodur®§, which is an LTE glass-ceramic, is also currently under evaluation.

The functional needs for high resolution, low distortion imaging at ≤70nm CD without defects impose stringent requirements that push the state of

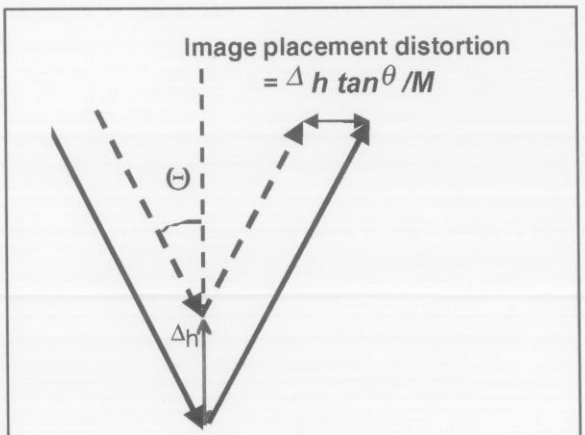


Figure 3: Non-telecentric illumination of the EUVL mask causes an image placement distortion when the substrate is not flat. Δh is the flatness non-uniformity, M is the magnification, and $\Delta h \tan\Theta / M$ is the image-placement distortion.

‡ ULE is a registered trademark of Corning, Inc., USA.
§ Zerodur is a registered trademark of Schott Glaswerk GmbH, Germany

the art in mask manufacturing. Ensuring the availability of an industrial supply base for key components and subsystems is crucial to the success of EUVL. It is essential to demonstrate that industry has a credible timeline for meeting EUVL requirements. As an early step toward meeting this goal, this paper serves to alert the mask supplier and mask metrology community of these EUVL requirements, to encourage industry participation in developing pertinent finishing, cleaning, and inspection technologies, and to highlight recent process improvements.

2. EUVL LOW-EXPANSION MASK SUBSTRATE REQUIREMENTS

2.0 Requirements of the EUVL mask for the ETS

Table 1 outlines our current requirements for EUVL mask substrates for use in the ETS, which will handle substrates in the shape of the 200mm silicon wafer with a notch. The establishment of a different SEMI standard format for production tools beyond the ETS is the subject of the Section 3 of this paper.

2.1 Mask shape and figure

The reflective nature of the EUVL mask means that the light must illuminate the mask at an off-normal angle, resulting in *non-telecentric illumination.* In the ETS this angle is 5–7° off normal. One of the consequences is that any non-uniformity in flatness would lead to an image-placement distortion at the wafer (Figure 3). Another driver of our flatness requirements is the designed range of operation of the ETS. During printing the mask is illuminated by a ring-field of radius 210mm and 6mm thickness (Figure 4). This ring field is scanned across an area that is 150mm long during printing. We define the *Quality Area* to be a rectangular area of 130mm x 110mm that encompasses the whole area to be printed, and the *Site Area* to be *any* rectangular sub-area of 16mm x 110mm inside the Quality Area that would completely enclose an area under illumination of the ring field. The ETS is designed to translate vertically the mask to keep the Site Area in focus and tilt the mask to correct for any linear slope of the illuminated area (Site Area) during printing. However the designed vertical ranges of travel are limited and a Global Total Indicator Reading (GTIR) of ≤1μm will be required. (GTIR is the smallest distance between two planes, both parallel to the least-squares reference plane for all points on the front surface of the mask.) Finally, any flatness non-uniformity of second order or higher in the Site Area cannot be compensated by tilting and may lead to an image placement distortion. We require that the SFSR, which is the flatness of any Site Area inside the Quality Area, to be ≤200nm.

Table 1. Shape, defect, and surface requirements of an EUVL mask for the Engineering Test Stand (ETS).

Total Wafer Characteristics	Metric Criteria
Figure Requirements	
Diameter	200 ± 0.02mm
Mean thickness	725 ± 15μm
Global Total Indicator Reading (GTIR)	≤ 2.0μm (within r < 90mm excl. zone)
TTV (Total Thickness Variation)	≤ 1μm m (within r < 90mm excl. zone)
SFSR (Quality Area= 130mm x 110mm Site Area= 16mm x 110 mm)	≤ 0.2μm (in any 16mm x 110mm Site Area inside Quality Area)
Surface Finish	
Front High Spatial Frequency Roughness (HSFR: $\lambda_{spatial} \leq 1\mu m$)	≤0.15nm rms
Front Mid-Spatial Frequency Roughness (MSFR: $10\mu m \geq \lambda_{spatial} > 1\mu m$)	≤0.2nm rms
Front side LPD (light-point defects) density	
Size ≥ 0.08 μm	≤ 3 LPD/wafer
Size ≥0.13 μm	≤ 1 LPD/wafer
Size ≥ 20 μm	None

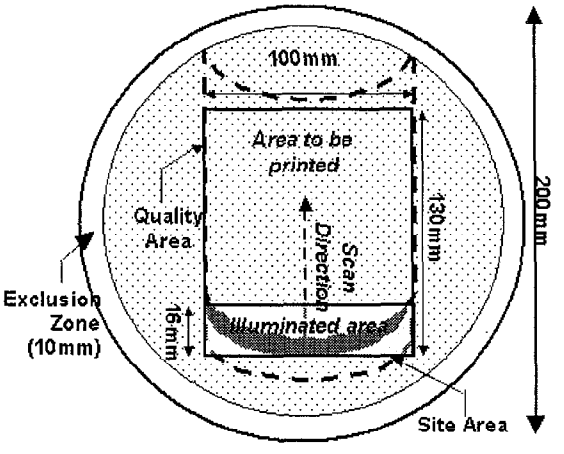


Figure 4. Quality Area and Site Area of the EUVL mask for the Engineering Test Stand (ETS).

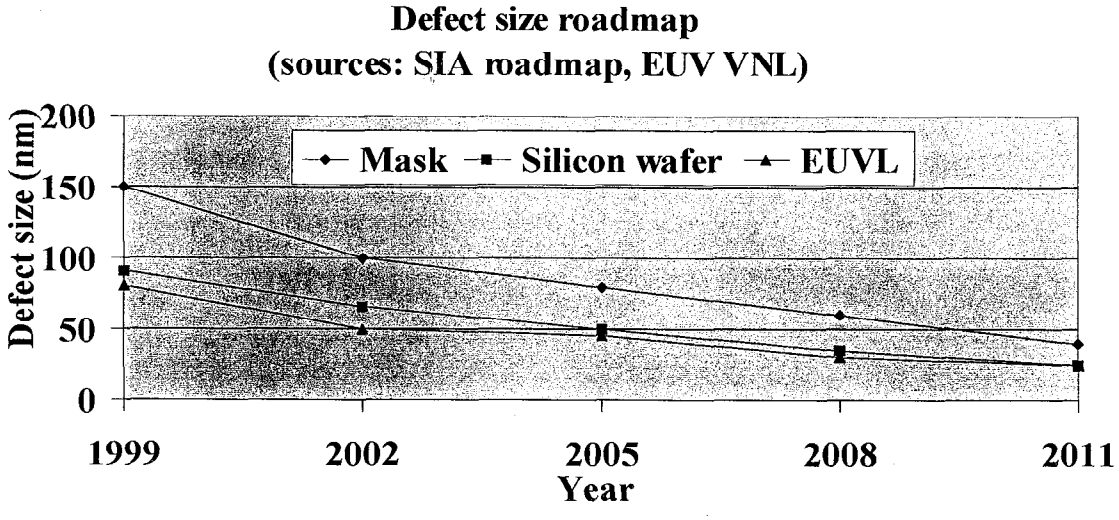


Figure 5. The EUVL mask defect size roadmap plotted against SIA defect size roadmap for silicon wafers and photomasks. The defect sizes for photomask are about double of those for silicon wafers (which current meet our needs). We need the mask suppliers and tool makers to bridge this gap to ensure that EUVL will be a success.

The mask substrate will be held with an electrostatic chuck on the ETS. The force of the chuck will be sufficiently strong such that any non-uniformity in substrate thickness will become height fluctuation on the front surface, causing an unacceptable image placement distortion. Our current specification for Total Thickness Variation (TTV) is ≤1μm.

2.2 Low-roughness finishing

The roughness requirements are divided into High Spatial Frequency Roughness (HSFR) and Mid-Spatial Frequency Roughness (MSFR). Roughness in each of the two regimes would have a different impact on printing. HSFR scatters light out of the entrance pupil and represents a loss of brightness, whereas MSFR leads to small angle scattering and results in image speckle[6]. The epi-silicon (100) wafers currently used as EUVL mask substrates have HSFR of ≤0.1nm. The requirements for LTE mask substrates will be ≤0.2nm rms for MSFR and ≤0.15nm rms for HSFR.

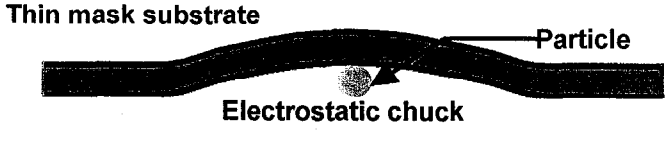


Figure 7: A thin substrate must be held with an electrostatic chuck because of the high stress in ML coating and gravitational sag. A pin chuck will not provide complete assurance that a particle or film on backside of mask will not deflect the front surface. A thicker substrate would be less prone to bulge and could also be mechanically held at the edges.

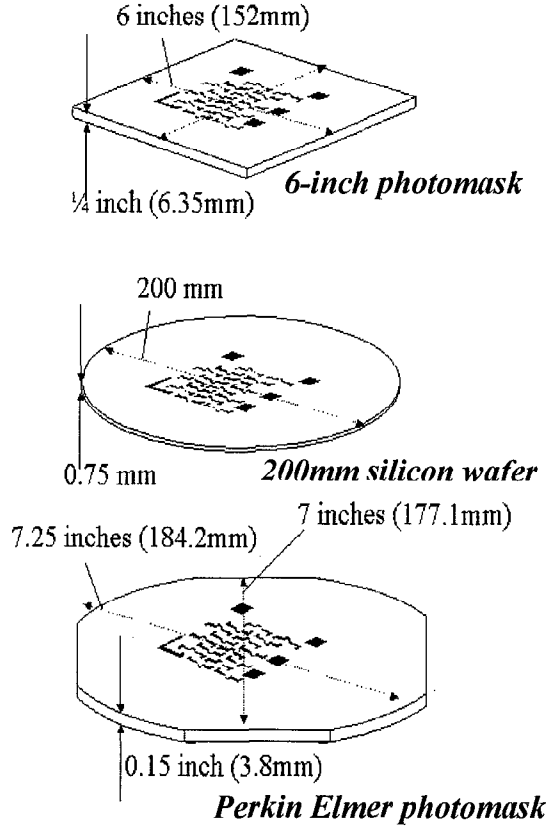


Figure 6. Three EUVL mask form factors under consideration for the SEMI standard.

2.3 Defect size and levels

Surface defects on the mask substrate may influence the ML coating topography. Defect reduction is the key challenge to mask fabrication. Although the current EUVL requirements for defects have been achieved on silicon wafers, they have not been achieved on quartz photomask substrates. The defect size roadmap for EUVL is plotted against the SIA defect size roadmaps for silicon wafers and photomasks in Figure 5, showing that the defect size for photomask is about 6 years behind or double that of silicon. Obtaining low defect mask substrate is crucial to the success of EUVL. We need the mask suppliers and tool makers to accelerate their development in cleaning and inspection to bridge this defect gap.

3. CHOICES FOR THE *SEMI* STANDARD FOR EUVL MASK FORMAT

In order for the tool makers to complete the designs of production tools to be ready for the 70nm node insertion, the format of the EUVL mask must be standardized. The EUVL mask format is driven by both the technical requirements of EUVL and the desire of the mask suppliers, tool makers, and end users to minimize the retooling of their existing infrastructure. Three form factors are under consideration (Figure 6): the 200mm diameter with 0.725mm thickness silicon wafer format, the 152mm (6-inch) wide with 6.35mm (_-inch) thickness standard photomask format, and the 7.25 inch diameter and with 3.81mm thickness Perkin Elmer photomask format.

The round shape of the silicon wafer format is conducive to higher uniformity in finishing and photoresist spin-coating and baking. More importantly, the silicon wafer format is compatible with wafer handling, cleaning, and inspection tools that are generally superior to comparable tools for photomasks. Indeed the original reason for choosing the silicon wafer as our substrate was to leverage these tools to produce EUVL masks with low defects. Consequently all the tools currently used or under construction in EUV VNL, including the ETS, are also geared for the silicon wafer format.

However, the silicon wafer format also presents a technical challenge that may be difficult to overcome beyond the 70nm node. The thin mask substrate cannot be

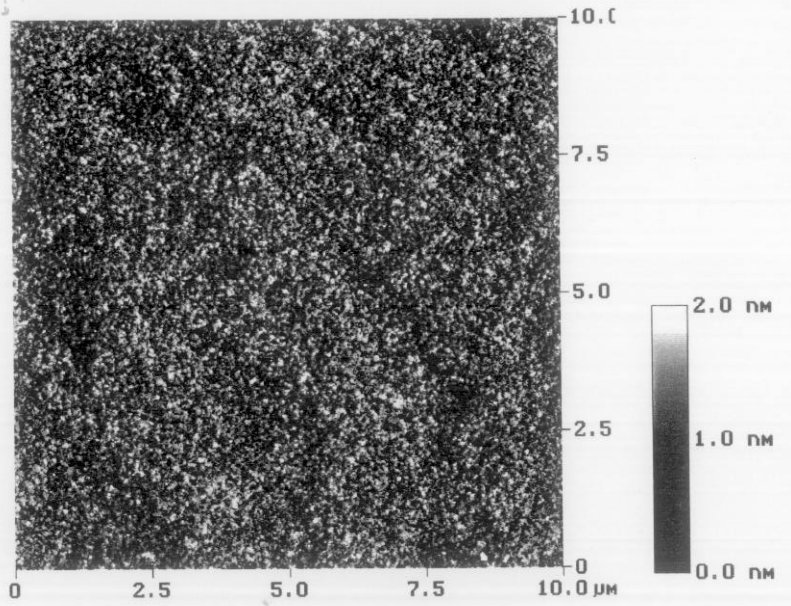


Figure 8: A 10µm scan of a ULE wafer produced by Company A, The MSFR of this topograph as measured by AFM is 0.35nm rms.

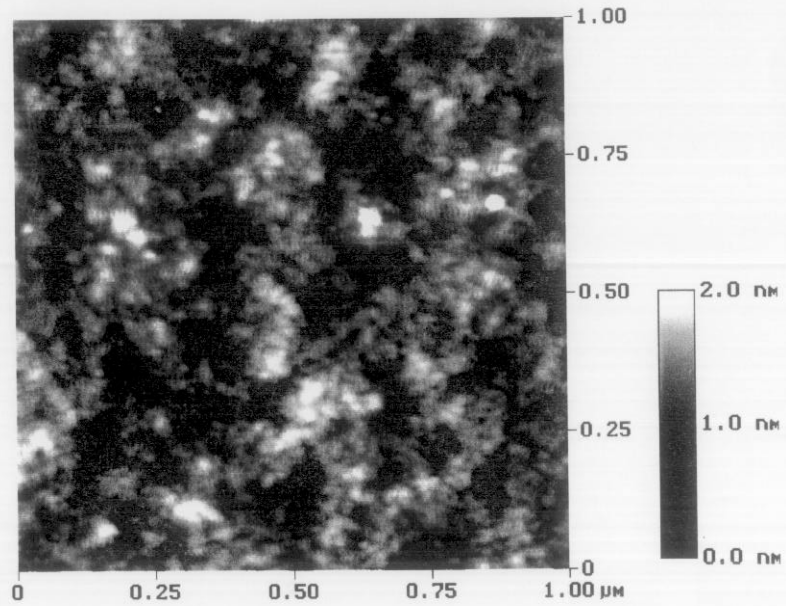


Figure 9: A 1µm AFM scan of the surface of a mask produced by Company A. The HSFR of this topograph as measured by AFM is 0.35nm rms.

mechanically held on the side because of bowing caused by the ML film stress and gravitational sag. This necessitates electrostatic chucking of the mask. When the mask is chucked during printing, a particle can potentially be trapped underneath a thin mask causing a bulge that may result in an unacceptable image-placement distortion (Figure 7).

Increasing the thickness would make the substrate more rigid. The particle will be embedded in the substrate. A thicker substrate will also have sufficient stiffness to be held mechanically on the side. Each of the other two thicker formats has its merits. The Perkin Elmer mask has straight edges and therefore does not require alignment marks. Its nearly round shape of the substrate allows for better spin-coating and baking uniformity. However, the use of this format is not presently widespread. On the other hand, the 6-inch photomask format is widely adopted and there already exists a large tooling infrastructure to support it. In March 1999, an *ad-hoc* committee was tasked to formulate a SEMI EUVL mask format. The first step was to carry out a survey of the opinion of the mask supplier and tool maker community on their opinions and concerns. The result of the survey revealed that a majority of the respondents favor the 6-inch photomask format.

4. PROGRESS OF MASK SUBSTRATE DEVELOPMENT OF INDUSTRIAL SUPPLIERS

The two main areas of the LTE mask substrate development that require significant effort are surface finishing (i.e. achieving low roughness) and low defect levels. Even though our surface-finish requirements are more stringent than those of today's photomasks, we believe from the start that they can be met with refinement to the current state of the art. The key challenge to EUVL mask finishing will be in achieving a low-defect count. Defect reduction research will be carried out in the next calendar year as we develop partnerships with current photomask and CMP suppliers and acquire inspection tools. Our current goal is to demonstrate that a clear path exists for achieving low roughness.

We have exploring three paths to obtain ULE® mask substrates. The three suppliers currently providing us with small quantities of samples for evaluation are a photomask supplier (Company A), a superpolishing vendor (Company B), and a CMP consumable supplier (Company C). Each company supplied at least two finished wafer substrates, which were inspected by our DI-7000 Atomic Force Microscope (AFM) at Lawrence Livermore National Laboratory. This activity will continue through the next year, with the expectation of increasing quality and quantities.

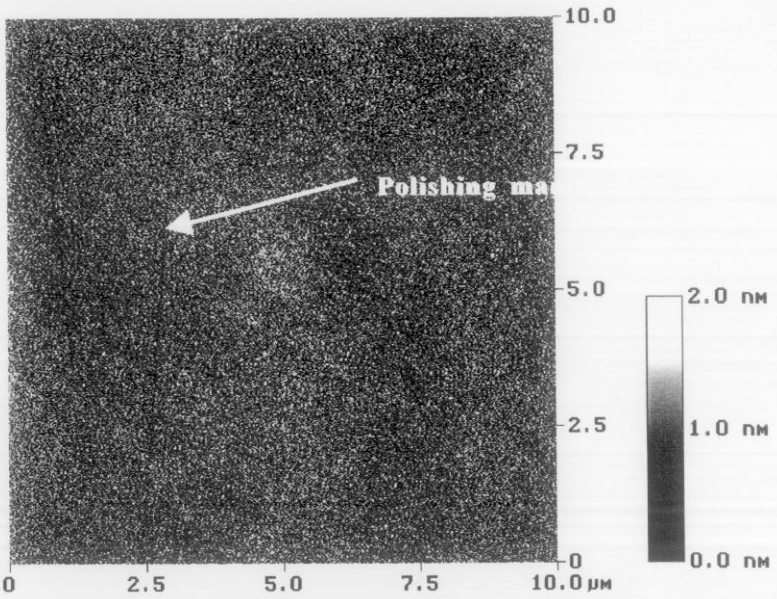


Figure 10: A 10µm scan ULE® substrate finished by Company B. The MSFR of this topograph as measured by AFM is 0.17nm rms. Sleeks such as those observed here were common on the substrate, but were all found to be less the 1.5nm in depth.

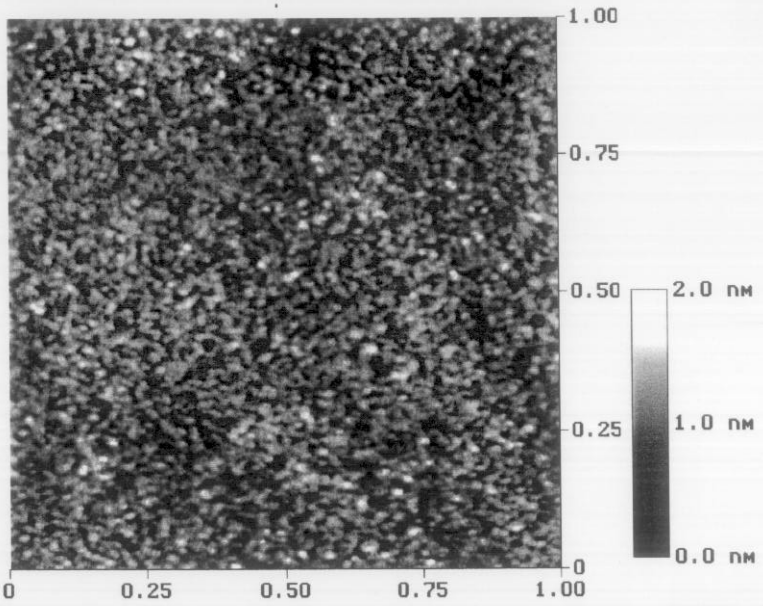
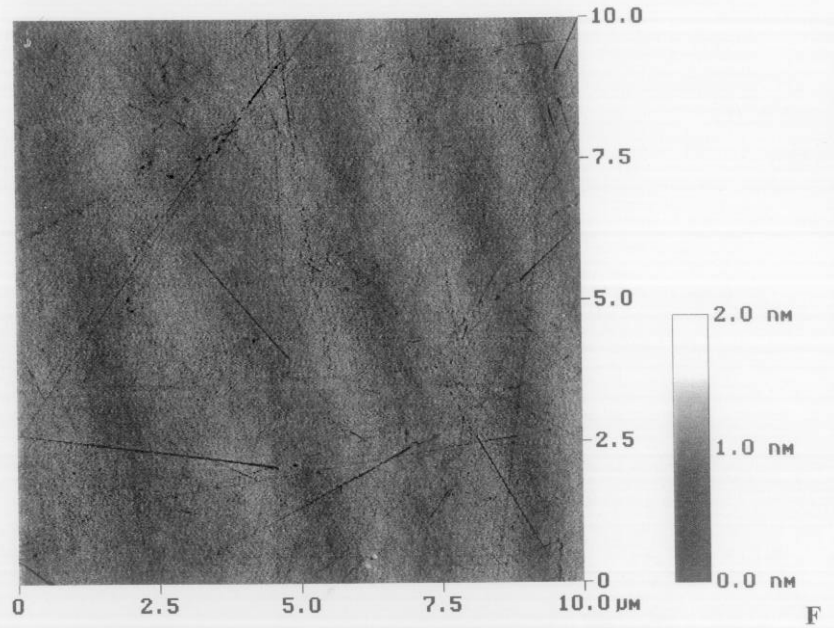


Figure 11: A 1µm scan ULE wafer from Company B with a HSFR of 0.21nm rms.

Company A provided samples that were produced at its optics polishing facility. We employed outside vendors to shape the ULE® boule to the right diameter, slice the boule into near-net thickness, and edge-round the individual wafers to the SEMI silicon wafer standard. The wafers were then lapped and finished by Company A. Figures 8 & 9 show AFM scans of 10μm and 1μm areas on one of the substrates. Overall we found the substrates to be of high quality, with average HSFR of 0.35nm rms and MSFR of 0.33nm rms. Although their mask substrates have the highest roughness of the three paths, they are also the most uniform, with no signs of sleeks or pits. We view this as an excellent first result.

Company B is a precision-optical finishing company that employs a proprietary finishing process to superpolish glass or glass-ceramic substrates that have MSFR and HSFR below 0.1nm rms. Although Company B does not have a semiconductor-production class cleanroom, we believe the substrates it produces had the best chance of meeting our roughness requirements. At Company B's request, we provided it with sliced ULE substrates only. Overall the substrate surfaces produced by Company B are much smoother than those produced by Company A (Figures 10 & 11). However, some polishing marks (sleeks and ridges) were clearly visible in the 10μm scans. The average MSFR and HSFR of the two substrates are 0.24 and 0.22nm rms, respectively. Both MSFR and HSFR very close to our requirements. We profiled about 10 of the sleeks and ridges and found them all to be less than 1.5nm in depth or in height.

Company C is a supplier of slurries and pads for the optical finishing and chemical mechanical polishing (CMP) industries. Its R&D facilities are geared for developing CMP processes for the semiconductor industry and can address the requirements of both low roughness and low defect levels. All of its CMP operations and metrology are carried out in a cleanroom and it possesses a comprehensive set of tools for cleaning, defect inspection, and surface finishing of the three companies evaluated. The substrates we provided to Company C had been shaped, sliced, and edge-rounded by the same vendors we have used to supply starting material for Company A. We further employed a lapping vendor to remove the subsurface



igure 12: A 10μm scan of a mask substrate produced by Company C, with MSFR of 0.14nm rms. The polishing marks were <1nm in depth on the average, although some were as deep as 5nm. We have traced the marks to the outside lapping vendor and corrected the problem.

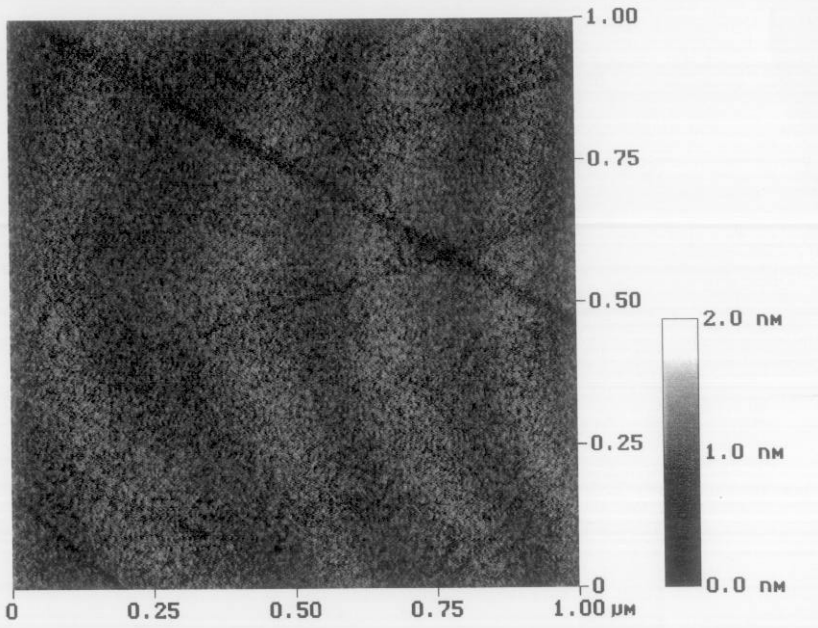


Figure 13: A 1μm scan of a mask substrate from Company C, with a HSFR of 0.13nm rms. The major sleek observed in this topograph is about 1nm in depth.

damage caused by the slicing. The lapped substrates were then shipped to Company C for final finishing.

The finished LTE mask substrates by Company C had the lowest roughness (Figure 12 and 13), which meet our requirements by having average MSFR and HSFR of 0.16 and 0.15nm rms, respectively. However, we also observed numerous discrete surface defects in the form of sleeks or pits on all of the AFM micrographs. Most of these defects were <1nm in depth, though several were as deep as 5nm. We hypothesized that the source of the defects was the lapping process and we have provided feedback to the outside lapping vendor who is using the information to produce a more uniform finish and low subsurface damage.

Overall, the substrates from the three companies have surface finishes that either meet and are close to meeting the stringent EUVL requirements of MSFR <0.2nm rms and HSFR <0.15nm rms. This confirmed our view that with refinement to the state of the art, the industry will be able to meet of surface-finish requirements in the near future.

5. SUMMARY

A significant effort is underway to develop the technology to produce LTE mask substrates for EUVL. We have engaged suppliers who are already producing substrates that meet or are close to meeting our surface-finish requirements. A SEMI standard for EUVL mask format is also being established as a first step to ensure that a mask and tool infrastructure will be in place by the 70nm node. However, the key challenge in mask substrate fabrication is *defect reduction.* Here the state of the art lags behind that of silicon wafers. To bridge this defect gap, accelerated development in LTE-substrate cleaning and inspection will be needed.

ACKNOWLEDGMENTS

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